UNIVERSITY EXAMINATIONS
2022/2023 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR TWO SEMESTER TWO EXAMINATIONS

FOR THE DEGREE OF
BACHELOR OF SCIENCE COMPUTER SCIENCE

COURSE CODE : CSC 222

COURSE TITLE : ADVANCED ASSEMBLY LANGUAGE AND MICROPROCESSORS

DATE: 19/ 04 /2023 TIME:9.00AM-11AM

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE (COMPULSORY) [30 MARKS]

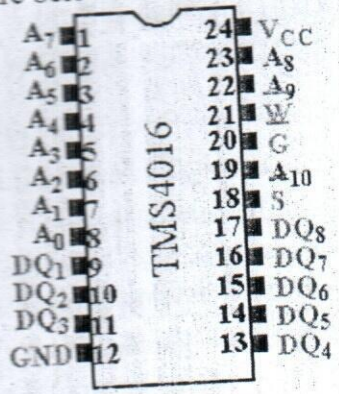
a) Highlight the significance of memory hierarchy. (3 marks)

b) Distinguish between source codes and object codes? (2 marks)

c) State the difference between the following categories of instructions:
   i) Arithmetic instructions and logical instructions (2 marks)
   ii) Machine control instructions and branching instructions (2 marks)

d) For each of the instruction below, state its category and write its hexcode:
   i) SUI 5EH (2 marks)
   ii) LDAX B (2 marks)
   iii) CM 4000H (3 marks)

e) The figure below shows a memory chip.



Determine:
   i) the number of address pins (1 mark)
   ii) the memory organization of the IC. (3 marks)
   iii) the address range of the chip (2 marks)

f) Write an ALP to subtract contents of memory 2010h from 2011h (5 marks)

QUESTION TWO [20 MARKS]

a) Highlight the functions of the following pins of 8085uP
   i) Reset out (2 marks)
   ii) INTR (2 marks)
   iii) READY (2 marks)
   iv) $\overline{INTA}$ (2 marks)

b) Dissemble each machine instruction below and state its task:
   i) C6H 45H (2 marks)
   ii) 21H, 00H, FFH (2 marks)
   iii) 0AH (2 marks)

c) Distinguish between an instruction format and instruction set (4 marks)

QUESTION THREE [20 MARKS]

a) Show the contents of the accumulator and the status of the flag bits after each of the following operations:
   i) 37H+46H (4 marks)
   ii) 50H + 50H – A0H (3 marks)
   iii) 78H-A9H (3 marks)

b) Write an assemble program to multiply a value 12H by 8 and provide output through port 80H. (10 marks)

QUESTION FOUR [20 MARKS]

a) Describe the stages of executing a POP D instruction in the microprocessor. (4 marks)

b) Below is a delay program.

```
        LXI B, 3400H
DELAY:  DCX B
        MOV A, C
        ORA B
        JNZ DELAY
        HLT
```

i) Given a clock frequency of 3MHz, calculate the duration of the delay program (7 marks)

ii) Write the algorithm of a delay program (5 marks)

iii) Convert the assembly language of the delay program into hand code. (4 marks)

QUESTION FIVE [20 MARKS]

a) Draw a flowchart to illustrate a program that:

i. Reads a memory address 4200H
ii. set COUNTER to be equal to the read input
iii. decrements COUNTER to zero
iv. reads the next memory address and repeats steps (ii) to (iv) (8 marks)

b) Write a ALP program for part (a) above. (12 marks)

INSTRUCTION SET OF 8085

HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL
00	NOP	25	DCR H	4A	MOV C, D	6F	MOV L, A	94	SUB H	B9	CMP C	DE	SBI D8
01	LXI B, D16	26	MVI H, D8	4B	MOV C, E	70	MOV M, B	95	SUB L	BA	CMP D	DF	RST 3
02	STAX B	27	DAA	4C	MOV C, H	71	MOV M, C	96	SUB M	BB	CMP E	E0	RPO
03	INX B	28	-	4D	MOV C, A	72	MOV M, D	97	SUB A	BC	CMP H	E1	POP H
04	INR B	29	DAD H	4E	MOV C, M	73	MOV M, E	98	SBB B	BD	CMP L	E2	JPO Adr
05	DCR B	2A	LHLD Adr	4F	MOV C, A	74	MOV M, H	99	SBB C	BE	CMP M	E3	XTHL
06	MVI B, D8	2B	DCX H	50	MOV D, B	75	MOV M, L	9A	SBB D	BF	CMP A	E4	CPO
07	RLC	2C	INR L	51	MOV D, C	76	HLT	9B	SBB E	C0	RNZ	E5	PUSH H
08	-	2D	DCR L	52	MOV D, D	77	MOV M, A	9C	SBB H	C1	POP B	E6	ANI D8
09	DAD B	2E	MVI L, D8	53	MOV D, E	78	MOV A, B	9D	SBB L	C2	JNZ Adr	E7	RST 4
0A	LDAX B	2F	CMA	54	MOV D, H	79	MOV A, C	9E	SBB M	C3	JMP Adr	E8	RPE
0B	DCX B	30	SIM	55	MOV D, L	7A	MOV A, D	9F	SBB A	C4	CNZ Adr	E9	PCHL
0C	INR C	31	LXI SP, D16	56	MOV D, M	7B	MOV A, E	A0	ANA B	C5	PUSH B	EA	JPE Adr
0D	DCR C	32	STA Adr	57	MOV D, A	7C	MOV A, H	A1	ANA C	C6	ADI D8	EB	XCHG
0E	MVI C, D8	33	INX SP	58	MOV E, B	7D	MOV A, L	A2	ANA D	C7	RST 0	EC	CPE Adr
0F	RRC	34	INR M	59	MOV E, C	7E	MOV A, M	A3	ANA E	C8	RZ	ED	-
10	-	35	DCR M	5A	MOV E, D	7F	MOV A, A	A4	ANA H	C9	RET Adr	EE	ERI D8
11	LXI D, D8	36	MVI M, D8	5B	MOV E, E	80	ADD B	A5	ANA L	CA	JZ	EF	RST 5
12	STAX D	37	STC	5C	MOV E, H	81	ADD C	A6	ANA M	CB	-	F0	RP
13	INX D	38	-	5D	MOV E, L	82	ADD D	A7	ANA A	CC	CZ Adr	F1	POP PS
14	INR D	39	DAD SP	5E	MOV E, M	83	ADD E	A8	XRA B	CD	CALL Adr	F2	JP Adr
15	DCR D	3A	LDA Adr	5F	MOV E, A	84	ADD H	A9	XRA C	CE	ACI D8	F3	DI
16	MVI D, D8	3B	DCX SP	60	MOV H, B	85	ADD L	AA	XRA D	CF	RST 1	F4	CP A
17	RAL	3C	INR A	61	MOV H, C	86	ADD M	AB	XRA E	D0	RNC	F5	PU

HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL	HEX	AL
18	-	**3D**	DCR A	**62**	MOV H, D	**87**	ADD A	**AC**	XRA H	**D1**	POP D	**F6**	ORI D8
19	DAD D	**3E**	MVI A, D8	**63**	MOV H, E	**88**	ADC B	**AD**	XRA L	**D2**	JNC Adr	**F7**	RST 6
1A	LDAX D	**3F**	CMC	**64**	MOV H, H	**89**	ADC C	**AE**	XRA M	**D3**	OUT D8	**F8**	RM
1B	DCX D	**40**	MOV B, B	**65**	MOV H, L	**8A**	ADC D	**AF**	XRA A	**D4**	CNC Adr	**F9**	SPHL
1C	INR E	**41**	MOV B, C	**66**	MOV H, M	**8B**	ADC E	**B0**	ORA B	**D5**	PUSH D	**FA**	JM Adr
1D	DCR E	**42**	MOV B, D	**67**	MOV H, A	**8C**	ADC H	**B1**	ORA C	**D6**	SUI D8	**FB**	EI
1E	MVI E, D8	**43**	MOV B, E	**68**	MOV L, B	**8D**	ADC L	**B2**	ORA D	**D7**	RST 2	**FC**	CM Adr
1F	RAR	**44**	MOV B, H	**69**	MOV L, C	**8E**	ADC M	**B3**	ORA E	**D8**	RC	**FD**	-
20	RIM	**45**	MOV B, A	**6A**	MOV L, D	**8F**	ADC A	**B4**	ORA H	**D9**	-	**FE**	CPI D8
21	LXI H, D16	**46**	MOV B, M	**6B**	MOV L, E	**90**	SUB B	**B5**	ORA L	**DA**	JC Adr	**FF**	RST 7
22	SHLD Adr	**47**	MOV B, A	**6C**	MOV L, H	**91**	SUB C	**B6**	ORA M	**DB**	IN D8		
23	INX H	**48**	MOV C, B	**6D**	MOV L, L	**92**	SUB D	**B7**	ORA A	**DC**	CC Adr		
24	INR H	**49**	MOV C, C	**6E**	MOV L, M	**93**	SUB E	**B8**	CMP B	**DD**	-		