UNIVERSITY EXAMINATIONS
2023/2024 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR THREE SEMESTER ONE EXAMINATIONS

FOR THE DEGREE IN
(COMPUTER SCIENCE)

COURSE CODE : CSC315

COURSE TITLE : COMPUTER ARCHTECTURE II

DATE: 13/12/2023 TIME: 09:00 HRS – 11:00 HRS

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO

QUESTION ONE [COMPULSORY] [30 MARKS]

a) Using a diagram explain the computer memory hierarchy considering speed of access, capacity and pricing. [4 Marks]

b) Discuss the concept of Memory interleaving and give its advantages [5 Marks]

c) Each instruction must contain the information required by the CPU for execution. Each instruction format consists of two components. State and explain the components [4 Marks]

d) State four differences between RISC and CISC [4 Marks]

e) Although instruction sets vary among machines, most of them include the same general types of operations. State and explain any three operations of instructions in a machine [6 Marks]

f) A computer must have a way of detecting the arrival of any type of input, what are these two ways [2 Marks]

g) Differentiate between SRAM and DRAM and with reasons state which one is suitable for making cache memory [5 Marks]

QUESTION TWO [20 MARKS]

a) Differentiate between programmed i/o and interrupt driven i/o stating which one has no bottleneck on CPU processing time [10 Marks]

b) Define cache write policy [4 Marks].

c) With brief explanation, describe any two types of Registers [6 Marks]

QUESTION THREE [20 MARKS]

a) Define RAID [2 Marks)

b) State and explain two types of control unit [4 Marks]

c) Describe the following terms as related to main memory [8 Marks]
   i. Temporal locality
   ii. Spatial locality
   iii. Sequential locality
   iv. Interleaved Memory

d) i. Define system bus [2 Marks]
   ii. Explain the any two types of system bus [4 Marks]

QUESTION FOUR [20 MARKS]

a) Describe the fetch execute cycle with the aid of a diagram [9 Marks]

b) When there is no space for a particular index in the cache, one of the two data values stored under that index will be replaced according to some predetermined replacement policy. State and explain any four replacement policy. [8 Marks]

c) State the three main components the Von Neumann Architecture [3 Marks].

QUESTION FIVE [20 MARKS]

a) To improve system performance, several design issues of the main von Neumann machine is to be put in place. This include CPU speed, faster memory and I/O devices, from the knowledge of computer architecture describe the design issues. [10 Marks]

b) i. What is bus arbitration [4 Marks]

ii. Explain the techniques of bus arbitration [6 Marks]