UNIVERSITY EXAMINATIONS
2022/2023 ACADEMIC YEAR

SPECIAL/SUPPLEMENTARY EXAMINATIONS
YEAR THREE SEMESTER TWO EXAMINATIONS

FOR THE DEGREE OF
BACHELOR OF SCIENCE COMPUTER SCIENCE

COURSE CODE : CSC 353E

COURSE TITLE : DIGITAL SYSTEM DESIGN

DATE: 09 /08/2023 **TIME: 11.00AM-1.00PM**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE (COMPULSORY) **[30 MARKS]**

a) Highlight the phases of digital system design (4 marks)

b) What is meant by the term 'Hardware Descriptive Language?' (2 marks)

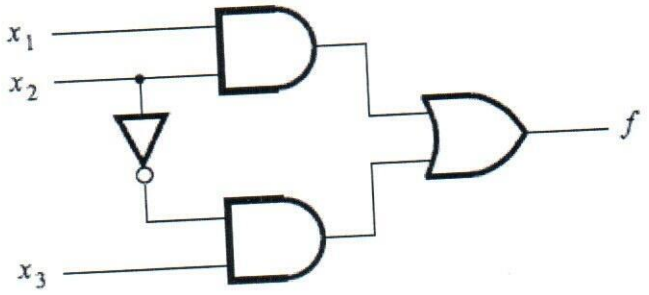
c) Discuss the usage of the following technologies in digital system design. (6 marks)

i) Standard cell Application Specific ICs

ii) Field Programmable Gate Arrays

iii) Custom-chip

d) Write a VHDL entity and architecture declaration of the circuit below: (7 marks)



e) Develop a truth table of a process statement below (3 marks)

```
PROCESS ( Sel, x1, x2 )
BEGIN
        IF Sel _'0' THEN
                f <=x1 ;
        ELSE
                f <=x2 ;
        END IF ;
END PROCESS
```

f) Write a VHDL code of a circuit represented by the function below: (8 marks)

$$f(x_1, x_2, x_3) = \Sigma m(0, 2, 4, 5, 6)$$

SECTION B

QUESTION TWO

a) Highlight six considerations in the design process (6 marks)

b) Define the term synthesis in HDL and outline its phases (8 marks)

c) Write a VHDL code of a circuit represented by the function: (6 marks)

$$f(x_1, x_2) = \bar{x}_1\bar{x}_2 + \bar{x}_1x_2 + x_1x_2$$

QUESTION THREE

a) Describe the following costs in design (6 marks)

i) Non-Recurrent Engineering cost

ii) Part-cost

iii) Time-to-market cost

b) Below is a truth table of a 4-to-1 multiplexer which has x0, x1, x2, x3 and s as input signals and f as output signal.

Input, s	Output, f
x0	00

x1	01
x2	10
x3	11

i) Draw a behavioural view block diagram for the multiplexer (4 marks)

ii) Write a completed VHDL program that assigns signals using WITH _ SELECT_WHEN clauses (10 marks)

QUESTION FOUR

a) Distinguish HDL programming from normal software languages (4 marks)

b) Explain the following terms as used in Gate implementation: (4 marks)

i) Noise margin

ii) Propagation delay

iii) Fan-out

iv) Cost of a gate

c) Write the VHDL code of a 4-to-2 priority encoder using the IF_THEN_ELSE clauses to meet the specification of the truth table below: (12 marks)

inputs				outputs		
x_1	x_2	x_3	x_4	y_1	y_2	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	x	1	0	1
1	x	x	x	1	1	1

QUESTION FIVE

a) Describe the details of the following phases; design entry, synthesis, functional simulation, physical design, timing simulation and chip configuration, of a typical Computer Aided Design system for developing the logic circuit (10 marks)

b) Write a VHDL code for a 2-to-4 decoder using the CASE_WHEN_OTHERS statements to implement the truth table. x_1 and x_2 are the data inputs. En is the enable input (10 marks)

inputs			outputs			
En	x_1	x_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	1	1	0
1	1	1	1	0	0	0
0	x	x	0	0	0	0